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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Steven Fischman, ESQ.
Scully, Scott, Murphy and Presser
400 Garden City Plaza
Garden City, NY 11530

EXAMINER	
PADGETT, MARIANNE L	
ART UNIT	**PAPER NUMBER**
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,647	CHOE ET AL.	
	Examiner	Art Unit	
	Marianne L. Padgett	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s)_____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The examiner notes that the **declaration under 37 CFR 1.131** submitted on 10/15/2007 is unsigned (the examiner notified applicants of this in a telephone message on 10/18/07), and as of 12/20/2007 has not been replaced by a signed copy, hence **will not be considered**, as it has not been properly executed.

2. The four **terminal disclaimers** submitted 10/15/2007 over PN 6,800,518, PN 6,486,037, SN 10/674,648 & SN 11/164,632, have been **approved**, thus **removing** the **obviousness double patenting** rejections of sections 8-9 & 11-12 of the action mailed 6/14/07.

Applicants' amendments to the claims have corrected the 112, second paragraph problems noted in section 1 of the action mailed 6/14/2007, thus removing the 112, second rejection.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly

owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-9, 13-16 & 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda Tadashi (JP 09-064323; also see Patent Abstracts of Japan & 2 machine translations), discussed in sections 4 & 5 of the action mailed 6/14/2007.

In the paragraph bridging page 6-7 in their response of 10/15/2007, applicants point out that there independent claims 1, 23 & 24 recite "an oxygen dose of about 1E17 atom/cm^2 or less", noting that in [0004] of Tadashi, an oxygen ion beam as of 1E18/cm^2 is given, although the examiner notes what the translations actually give oxygen ion injection rates in [0004] as "1018-/cm2", but as [0004] of the actual Japanese patent document contains "$10^{18}/cm^2$", applicants' assessment of this exemplary teaching is considered correct. However, the obviousness of values in the claimed range inclusive of about 1E17 atom/cm^2, has already previously been discussed (thus is not a new issue), particularly with respect to the previously cited [0017], which also discusses oxygen ion dose, teaching a basis for optimizing the amount of oxygen ion implantation, where it is suggested that an exemplary useful amount for oxygen ion implantation is on the order of $10^{18}/cm^2$ (interpretation confirmed by Japanese translator), with the examiner further noting that "on the order of" includes values both greater & less than the specifically recited value, while applicants' endpoint of " about 1E17 atom/cm^2" includes values greater than the specifically recited value, hence while it is arguable whether on the order of $10^{18}/cm^2$ & about 1E17 atom/cm^2 could be considered to be overlapping ranges, the examiner maintains as previously discussed, that the claimed values are obvious variations on the teachings of Ikeda Tadashi. The examiner notes that applicants only argue why "1E18 atoms per square centimeter oxygen dose is greater than an upper limit

of 1E17 atoms per square centimeter oxygen dose" (page 7 of 10/15/07 response) prevents Ikeda Tadashi from being a 102(e), does not discuss the effect of "about" & does not discuss why the claimed values would not be obvious as previously set forth, nor provide any showing of a significantly different or unobvious result from use of this variation in dosage.

It was previously noted that in applicants' specification in paragraph [0026], they redefined the phrase "Si-containing", which has a plain meaning of anything containing silicon, to have the narrower meaning of "a semiconductor material that includes at least silicon".

Ikeda Tadashi teaches employing a semiconductor substrate, that may be a silicon wafer, which has been doped to be either n-type or p-type, and treating it with a HF solution, with an exemplary current density of 10-80 mA/cm^2 creating a porous silicon layer of a desired thickness (~ 100 nm exemplified) via anodization (figures 1 (a-b) & 2 (a-b); [0004]; [0015-17]; [0022] & [0027]). Thereafter, a single crystal silicon layer is deposited over the porous silicon layer, then oxygen ions are implanted through the single crystal silicon layer into the porous silicon layer, after which treatment is performed at temperatures of 1200-1350°C, so as to form an "embedded oxide film layer" from the ion implanted porous layer, which due to the overall oxidation processing technique is taught to not increase in volume from that of the original porous layer. Options of uniformly ion implanting or using a patterned resist to mask areas during ion implanting, with potentially multiple ion implantings are taught (figures 1 (c-e) & 2 (c-e); [0017-19] & [0022-25]). Ikeda notes that their techniques solve problems discussed with respect to the conventional processes illustrated in figures 3 & 4.

While Ikeda Tadashi teaches creating a porous layer (≡ porous Si-containing region), the percentage of that layer which is porous is not disclosed, however at the claimed range of "about 0.01 % or greater" is so broad that it covers virtually any conceivable amount that may be produced by Ikeda's process & still be called porous. Furthermore, the anodization technique used by Ikeda to create the porosity is essentially the same as the anodization process claimed by applicants & discussed in

applicants' specification on [0029-32] as used to convert doped a single crystal silicon to porous silicon, thus like porosities would have been expected to have inherently been produced from like processes & materials. Alternately, it would've been obvious to one of ordinary skill in the art to create sufficient porosity in order to effect Ikeda's taught process of creating an embedded or buried oxide layer, where volume increase is not a problem (i.e. avoid crystal & stress defects caused by increased volume during oxidation), such that the compositional parameters, such as degree of doping & the HF anodization parameters would have been optimized based on those taught in order to produce required porosity for required effects.

Ikeda Tadashi does not teach that the claimed ion dose of "from about 1E16 to about 1E17 atoms/cm^2", however they do teach optimizing the volume ratio between the Si:O to about 1:2, and that in their particular example the amount of oxygen implanted was about 10^{18}. It would've been obvious to one of ordinary skill in the art to optimize the dosage applied over the area being ion implanted dependent on the density of the porous area (i.e. more dense has more silicon, while less dense has less silicon, thus directly affecting the amount of oxygen needed to effect the ratio of Si:O) & the thickness of the buried oxide layer being for, as the thickness will also affect the amount of oxygen required to create the desired ratio for effective oxide formation in the oxygen ion implanted porous layer. Other ion implantation parameters, such as beam current, energy & temperature, are not discussed by Ikeda, however it would've been obvious to one of ordinary skill in the art to determine via routine experimentation such useful parameters for affecting the taught ion implantation, as they would be required to be determined in order to perform the taught process, where analogous parameters would have been expected, since analogous effects are being produced in like materials with like ions & analogous or overlapping structural results.

While Ikeda Tadashi teaches the heat treatment employing claim temperatures of 1200-1350°C, Ikeda does not discuss the atmosphere under which this heat treatment to create the embedded oxide layer is performed, however it would've been obvious to one of ordinary skill in the art that as one is creating

an oxide to employ atmospheres that have an oxygen ambient using a common source of oxygen, such as those claimed, where the atmosphere is otherwise unreactive or has no reaction that interferes with oxide formation (which would suggest to one of ordinary skill in the art use of inert gases to achieve desired pressure, prevent contamination, or like standard purposes), since such would have been expected to prevent out-gassing of oxygen, which could decrease the desired stoichiometry, & since performing oxidations under oxygen atmospheres is a standard procedure. It is noted that use of such an oxygen containing atmosphere during the heat treatment process/annealing would inherently affect the surface of the single crystal silicon layer to affect thermal oxidation thereon, and as such would be further desirable for particular device formation sequences which require such a surface oxide layer.

5. Claims 1-15 & 18-25 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Houston et al. (2002/0086463 A1), as discussed in section 6 of the action mailed 6/14/2007.

In their arguments in the paragraph bridging pages 7-8 applicants state "that Houston at paragraph 0016 teaches that the thickness of the porous layer may be in a range of **nanometers** to microns, which is indicative of a greater thickness than the nanometers thickness proposed by the examiner. Since a thickness in a micron range is greater than the '100 nm or less' thickness recited by applicant..." (emphasis added), which statement must be considered inaccurate, illogical or mistaken, as a range of thicknesses including nanometer thicknesses cannot be said to be indicative of thicknesses that are only in the micron range, which would be one interpretation of what applicants appear to be trying to say. Alternatively, if applicants are trying to argue that the teachings of Houston include values larger than applicants claim, this is not convincing because the nanometer values taught to be useful by Houston may be inclusive of those taught be useful by applicants and are clearly not restricted to microns, since teaching values excluded by applicants' claims, does not negate alternative teachings that are included by applicants claims. Applicants have provided no convincing arguments concerning why one should disregard the nanometers teaching from Houston's generic range, only consider the microns, nor in view

of the previously presented obviousness arguments, why one would not consider in the range of nanometers to include 1-100 nm, or why one should considered this part of the range that may be considered obviously encompassed by Houston's generic teaching to be patently significantly different than any other part of Houston's range.

As previously discussed, Houston et al. teach making an silicon-on-insulator (SOI) wafer, where a first layer of porous silicon is formed by anodizing a boron (i.e., p-type) doped silicon wafer using a HF solution, such that the depth of the porous silicon is controlled by the timing of the anodization treatment or by limiting the depth of the boron doping, where thicknesses in the range of nanometers to microns can be obtained ([0006]; [0016]). Houston et al. teach that the anodizing process can result in cracks on the surface of the porous silicon, hence they employ a "prebake" process that fills up surface pores with migrated silicon atoms in order to reduce the surface energy. This "prebake" process seals the surface; may employ a hydrogen ambient; and the sealed surface may provide a starting point for subsequent epitaxial growth of a layer on the surface, where the quality of the epitaxial layer may depend on the surface pore filling during the sealing bake ([0006]; [0018-19]; [0022]). The epitaxial semiconductor layer may be deposited on the sealed surface either before or after oxygen ion implanting, where the ion implanting may be carried out via plasma oxygen implant or other oxygen implanting methods, with the oxidizing species derived from molecular oxygen or other sources, such as ozone or N_2O, and where oxygen doses may be on the order of 10^{17}-10^{18} oxygen ions per cm^2, which overlaps with claimed dosages ([0006]; [0016]; [0020]; 0023-25] & [0031]). The oxidation process, which forms the buried oxide layer from the implanted oxygen is completed by high-temperature anneal, which appears to use temperatures on the order of 1000°C for about 30 minutes ([0006] & [0020]). Houston et al. teach their process provides a number of advantages ([0007-11]), inclusive of aiding a planarity, sharp definition of the oxide layer, etc.

The teachings of Houston et al. differ from the present claims by not providing a specific thickness for the porous layer or the resultant buried oxide layer produced by its oxygen implantation & anneal, however as Houston et al. teach means for controlling the thickness of the porous layer, hence the buried oxide layer, suggesting its thickness measurements can be in the range of **nanometers**, it would have been obvious to one of ordinary skill in the art that contemplated thicknesses for the buried oxide layer include thicknesses as claimed of about 100 nm or less, as the teachings of nanometer range is suggestive thereof & as the intended use relates to integrated circuit structures where such thicknesses would have been considered typical for typical desired miniaturization of circuit designs.

Houston et al. did not provide claimed parameters for current densities for the anodization process nor for the ion implantation process, nor ion beam energy as for implantation, nor temperatures for baking to seal the porous surface in the hydrogen ambient, however given the taught process of Houston et al., one of ordinary skill in the art would have been expected to employ routine experimentation to determine necessary parameters not explicitly given, such as current densities, energies & temperatures, in order to employ the taught procedure to produce the taught results, which would have been expected to be inclusive of claimed ranges, as no critical differences seen in their effects from those claim. Note that Houston et al.'s teaching of the implanting oxygen with plasma or other ion implantation methods, would have been suggestive to one of ordinary skill in the art of oxygen plasmas or oxygen ion beams to effect the oxygen implantation, where the parameters of either technique would have been optimized to produce doses on the order claim, noting that in paragraph [0006] Houston et al. teach implantation of low oxygen doses, and that the 10^{18} O ions/cm^2 is considered to be a relatively heavy dose [0020], which teachings would suggest to one of ordinary skill an apparent preference for the lower end of the taught dosage range.

It is noted that while Houston et al. has much discussion on growing of an epitaxial layer (epi layer), its material is generally not identified, although [0023 & 25] refers to it as an epitaxial

semiconductor layer, but [0024] in the same sequence only refers to a semiconductor layer, not mentioning epitaxial, while [0006] also does not discuss an epitaxial layer in the process sequence, instead discusses forming a thin silicon film by standard deposition techniques on the sealed porous silicon layer, hence growth of an epitaxial silicon layer on the sealed H-prebaked surface is considered taught or suggested by Houston et al., or alternatively obvious due to the overlapping of the teachings for the desired deposit on the sealed surface as presented above.

6. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bendernagel et al. (6,800,518 B2, which incorporates PN 5,930,643 to Sadana et al. by reference), as discussed in section 7 of the action mailed 6/14/2007.

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicants have not met the above stated criteria, nor have they presented any other arguments to overcome this rejection with respect to by Bendernagel et al. (6,800,518 B2).

As previously discussed, Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & buried void plane structures, by forming a layer of porous silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current (~0.1-20 mA/cm^2) & voltage (~0.1-10 volts typical, ~0.5-5 volts preferred) used, the HF concentration, and the dopant type & concentration in the wafer, and where thickness of the porous silicon layer may additionally depend on the time (~30 sec.-10 min.,~1-5 min.

more highly preferred) of anodization process. For this process Bendernagel et al. teach that the "semiconductor **wafer needs to be doped**, preferably but not necessarily with **p-type** doping atoms. When a **boron**-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about 1E15 to about 1E19 atom/cm^3..." (emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about 1E16-2E18 atoms/cm^2, implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm^2, and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given (~5E16-2E17 atoms/cm^2, ~150-300 KeV, ~1.0-10 mA/cm2, ~550-600°C) as well as this high-temperature ion implantation step followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s) high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into buried void layers or buried conductive regions. The high-temperature annealing in is performed at temperatures of about 1300°C or greater, but less than the melting point of Si , which is 1415°C, and may be carried out it atmospheres of pure oxygen

(O_2), oxygen mixed with an inert gas or N_2, or either without oxygen, or vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a post hydrogen annealing process, which may use the same or different conditions (0.25-3 hours, $\leq$ 82 Torr H-ambient, T = 1100-1150°C) is then employed. Col. 9, lines 7-12 note that during annealing the porous silicon is consumed by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bendernagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be controlled by adjusting vertical depth of the porous silicon layer form during HF-anodization and the dose of the implanted ions. Particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 84 doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically monocrystalline structure ≡ single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

With respect to applicant's claim 17, which is directed to specific parameters for a second oxygen implantation step, it is noted that Bendernagel et al's teachings on col. 8, lines 15-31 can be said to overlap with these parameters for their taught second implantation step at a normal room temperature, which is in the claimed temperature range for the second oxygen implantation, assuming that the other parameters employed for the second implantation can be any of the preceding taught parameters, which are overlapping with those claimed, or as suggested one may look at the exemplary art, such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via oxygen ion implantation, possibly through a capping layer, using a low-dose ion implantation (~≥5E16) at high temperatures about

≥ 200°C, plus a second yet lower ion dose implantation at same or different energies carried out at cryogenic temperatures to about 300°C at doses of about 2E14-4E15 ion/cm^2. The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient (N_2 or Ar) mixed with oxygen at temperatures from about 1300°C or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), thus providing specific parameters for the two-step oxygen ion implantation alternative, which read on claim parameters and which are employed with oxidation & annealing procedures as taught and claimed.

7. Claims 1 & 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sadana et al. (5,930,643), which was discussed above in section 6 & previously in sections 7 & 8 of the action mailed 6/14/2007.

Applicants have argued (page 8 of 10/15/07 response) that oxygen ion implantation does not expressly or inherently caused voids in semiconductor substrates, but may provide amorphization, however their claims do not necessarily require voids to be produced, as voids are claimed in the alternative with "vacancies", which one of ordinary skill in the art would clearly consider to be encompassed by the taught defects or damaged regions of Sadana et al. (643), as was previously discussed & not contradicted by applicant's arguments, and as vacancies are a type of defect or damage inherently caused by ion implantation, thus considered to be equivalent concepts or semantics differences. Applicants have provided no arguments, nor evidence that would contradict this, nor have they amended their claims to limit them to necessitating voids, which is the only option they discuss in their arguments. When alternatives are claimed, only one of the alternatives need be taught for a reference to read on the claim. Note, should the claims be limited to voids, the obviousness of voids with respect to Sadana et al. (643) will need to be considered, but remains presently considered superfluous in view of remaining pending grounds rejection.

As noted above & previously, Sadana et al. (643) has all the parameters to the claimed oxygen ion implanting & annealing steps, for producing buried oxide layers of thicknesses claimed. While Sadana et al. does not discuss providing a silicon-containing semiconductor material in the substrate that has a region with "vacancies or voids located therein" the initial ion implanting step which creates **defects with inherently include defects that may be described as "vacancies",** as created defects would have been expected to include displacements of atoms in the silicon-containing substrate, thus vacancies. Further note that while Sadana et al. (643) most explicitly discuss a 2-step procedure, their teachings are inclusive of "this low temperature/low dose ion implantation step may be carried out in either a single step with a single temperature or multiple steps with multiple temperatures, which range from about cryogenic to about 300°C or less", such that the multistep ion implantation procedure described thereby reads on applicant's claimed process, even if one considers the "providing..." step necessarily separate from the step of "implanting...", as the multistep sequence to produce the low temperature low dose implantation, encompasses or overlaps with those sets of applicants' oxygen ion implantation parameters.

As previously discussed, claimed temperatures for two oxygen ion implantations relate to Sadana et al. (discussed above in section 6), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (buried **damage region** & **adjacent amorphous** layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the **defect containing amorphous region** is believed to enhance oxygen diffusion into the silicon & combine with the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence noting claimed parameters & claimed multiple ion implantations as discussed in Sadana et al. for taught advantages in

producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques. Also note that exemplary buried oxide region thicknesses via Sadana et al.'s process include 1000 Angstroms, i.e. 100 nm (example 1, specifically col. 7, lines 60-62), relate to claimed thicknesses for buried oxide layers in semiconductor substrate constructions.

8. It remains noted that, Sadana et al. (6,222,253 B1) is cited as substantially equivalent to Sadana et al. (643), for purposes of the rejection, except that it only discusses the two-step ion implantation sequences, with analogous subsequent annealing steps, rather than also discussing the option multiple lower temperature & dose oxygen ion implantations subsequent to the initial oxygen ion implantation (summary, especially col. 2, lines 49-col. 3, lines 7; & col. 4, line 10-col. 5, lines 37). However it is particularly noted that Sadana et al. (253) substantiates the above arguments of including "vacancies" as types of defects created in the initial oxygen ion implantation step, since in col. 4, lines 40-49 oxygen ion implantations in doses of $(3\text{-}5)10^{17}$ ion/cm^2 are explicitly taught to cause "Si damage clusters of Si atoms, Si in interstitial locations and Si vacancies with and/or without oxygen".

Roitman et al. (6204546 B1: abstract; summary; col. 2, lines 44-col. 4, lines 24) has substantially equivalent disclosure to Sadana et al. ((253) or (643)) for purposes of the rejection, except is more similar to (253) & teaches at the first ion implantation creates "silicon crystal and defect regions having stacking faults and dislocation defects" (col. 2, lines 56-57), where dislocation is considered to be substantially equivalent to vacancies, and discusses buried oxide layer thicknesses in the range of 300-800 Angstroms (i.e. 30-80 nm).

9. Claims 1 & 12-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Norcott et al. (6,486,037 B2, which is the child of PN 5,930,643 to Sadana et al & contains essentially the same teachings with respect to the claims as written), as previously discussed in section 11 of the action mailed 6/14/2007.

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

The above conditions have not been that & the arguments put forth with respect to Sadana et al. (643) above in section 7, are also applicable here.

10. Applicant's arguments filed 10/15/2007 & discussed above have been fully considered but they are not persuasive.

During updating of the search the following references to Minami et al. (2007/0215916 A1) & de Sousa et al. (2007/0164358 A1) were found to be of interest for discussion of relevant processing techniques (see claims), but are not prior art.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MLP/dictation software

12/20/2007

MARIANNE PADGETT
PRIMARY EXAMINER